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| EXAMINER | |
|---|---|
| STEELMAN, MARY J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2191 | |

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/066,061 | KALOGEROPULOS, SPIROS | |
| | Examiner | Art Unit | |
| | Mary J. Steelman | 2191 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9,11-26 and 28-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-26 and 28-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office Action is in response to Amendments and Remarks received 20 April 2005. Per Applicant's request, claims 1, 12, 19, 28, and 29 have been amended. New claims 30 and 31 have been added. Claims 10 and 27 have been canceled. Claims 1-9, 11-26, and 28-31 are pending. Per Applicant's request, the Specification has been amended.

### *Drawings*

2. Drawings are accepted by Examiner. Prior objections to drawings are hereby withdrawn.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-9, 11-26, and 28-31 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 5894576 to Bharadwaj.

Per claims 1, 28 and 29:

-method...system...computer program product...

(Bharadwaj teaches a method (col. 1, line 8), system (col. 3, line 33), and computer program product (col. 12, lines 30-45 – program storage device).)

-allocating registers;

(Bharadwaj teaches register allocation, as an example, (col. 4, lines 38-51) by using a register allocator.)

-building a trace comprising basic blocks;

(Bharadwaj teaches building a trace of basic blocks. Col. 3, lines 64-col. 4, line 8, a parser (trace input code), an intermediate representation builder and a code generator are used to generate a control flow diagram (trace comprising basic blocks) connecting basic blocks (col. 4, lines 6-10).)

-scheduling instructions within said trace after said allocating registers comprising:

(Bharadwaj teaches scheduling instructions (col. 4, lines 33-37). Bharadwaj teaches that scheduling may occur after allocating registers (col. 4, lines 48-51).

- moving a first instruction from a home block of said basic blocks to a destination block of said basic blocks;

  (Bharadwaj teaches moving a first instruction (col. 8, lines 59-61) from a data ready list (instruction from a home block) into a block (a destination block) and adding compensation code as necessary (col. 5, lines 50-52).)

- generating compensation code comprising:

(Bharadwaj teaches generating compensation code as necessary (col. 5, lines 24-27, col. 8, lines 61-63). See FIG. 9 and col. 10, lines 16-33. The scheduler determines if compensation code will be necessary and if so will insert the compensation code (col. 5, lines 45-52).)

- creating a compensation basic block;

(Bharadwaj teaches creating a compensation basic block at col. 5, line 24, "...insertion of an empty compensation basic block...")

- inserting a copy of said first instruction in said compensation basic block.

(Bharadwaj teaches inserting a copy of said first instruction in said compensation basic block at col. 5, lines 50-51, "compensation copy of the instruction...inserted into compensation block...")

Per claims 2 and 20:

- scheduling instructions comprises moving instructions between said basic blocks.

(Bharadwaj teaches scheduling instructions at col. 4, lines 33-37. Instructions are reordered (moved between basic blocks) by analyzing regions (col. 5, lines 1-3) of the control flow diagram and moving instructions between blocks within the region.)

Per claims 3 and 21:

-building a control flow graph comprising said basic blocks.

(Bharadwaj teaches building a control flow graph (col. 5, lines 2-3). Col. 5, lines 6-7, "...the region may...contain special blocks (comprising basic blocks)...")

Per claims 4 and 22:

-control flow graph comprises an off trace basic block.

(Bharadwaj teaches a control flow graph (col. 4, lines 8-9) with consideration given to successor blocks. Col. 6, lines 45-56, disclosed a control flow analyzer (trace control flow) while computing dominance, post-dominance, and control equivalence (successor and predecessor basic blocks) An off trace block may be the preceding or succeeding regions, that will subsequently be optimized. Since code is scheduled by region (col. 5, lines 1-3), an off trace block is also considered.)

Per claims 5 and 23:

-scheduling instructions comprises recognizing data dependencies from said off trace basic block.

(Bharadwaj teaches consideration given to data dependencies when scheduling instructions (col. 6, lines 57-63). See discussion in the rejection of claim 4 regarding 'off trace basic block.')

Per claims 6, 17, and 24:

-scheduling instructions comprises computing height information of said instructions.

(Bharadwaj teaches scheduling with consideration given to height information (col. 6, line 67).)

Per claims 7, 18, and 25:

-height information is computed using execution probabilities of said basic blocks.

(Bharadwaj teaches (col. 6, lines 64-67), "...the height of an instruction will affect its priority (execution priorities / probabilities).")

Per claims 8 and 26:

-said height information is computed using adjusted execution times of said instructions.

(Bharadwaj disclosed consideration to height information (col. 6, line 67- col. 7, line 6). An instruction height is related to the minimum number of cycles it takes to execute its associated chain of instructions (execution time).)

Per claim 9:

- scheduling instructions comprises computing an adjusted execution time of an instruction of said instructions by multiplying an execution time of said instruction by an execution probability factor.

(Bharadwaj disclosed computing an adjusted execution time by the block probability chosen to insert the instruction (col. 7, lines 1-15). An instruction in a high probability block will tend to have a grater priority than one in a low probability block. Instruction priority can also be adjusted during scheduling." An 'adjusted execution time' may be computed when determining the critical path of the block (col. 9, lines 35-48). A scheduler determines whether necessary compensation code would increase the execution time in an acceptable manner.)

Per claim 11:

- scheduling instructions comprises:

-building a trace block comprising said instructions;

(Bharadwaj disclosed scheduling instructions (FIG. 5, #54) and building a trace block comprising said instructions (col. 5, lines 1-15 – region builder partitions the program / a portion of the control flow diagram / may contain special blocks that represent...).)

-scheduling said instructions within said trace block;

(Bharadwaj disclosed scheduling within said trace block (FIG. 7, #82).)

-moving said instructions from said trace block to said basic blocks.

(Bharadwaj disclosed, using a control flow analyzer (FIG. 6, #66) moving instructions (col. 6, lines 42-43) from trace block (region control flow) to basic block actively being scheduled.)

Per claim 12:

A method comprising:

-allocating registers;

-building a trace after said allocating registers,

-said trace comprising basic blocks comprising instructions;

-building a trace block comprising said instructions;

-scheduling said instructions within said trace block;

-moving said instructions from said trace block to said basic blocks comprising:

-moving a first instruction from a home block of said basic blocks to a destination block of said basic blocks;

-generating compensation code comprising:

-creating a compensation basic block;

-inserting a copy of said first instruction in said compensation basic block.

(See limitations addressed in claims 1 and 11 above.)

Per claim 13:

- said building a trace block comprises inserting a join instruction into said trace block, said join instruction being a delimiter for a first basic block of said basic blocks.

(Bharadwaj disclosed inserting a 'join instruction' at col. 5, lines 15-27. Join blocks are handled by inserting an empty compensation block along the edge of a control flow graph where multiple predecessors exist. As such, it is a delimiter for a first basic block of said basic blocks, as following blocks flow through the join block, after flowing through the added compensation block. (Col. 5, lines 45-54) – This technique prevents redundant scheduling / execution of instructions.)

Per claim 14:

- updating a use set of said join instruction with a global live-in for an off trace basic block.

(Bharadwaj disclosed a control flow analyzer (col. 5, line 14) that handles (updating) join block instructions when analyzing control flow within a region (off trace basic block) , analyzing live global resources (col. 6, line 12 – fully use the machine resources). Additionally, (col. 6, lines 57-63) disclose a 'data dependence analyzer' which stores information related to 'global live-in' of register variables.)

Per claim 15:

- said global live-in is a set of registers which contain live values when entering said off trace basic block.

(Bharadwaj disclosed consideration to live values in registers when scheduling (col. 6, lines 11-13), "...if instructions were organized...so as to fully use the machine resources (registers)...nothing else could be scheduled..." Col. 4, lines 38-54 discloses the register allocator which determines which variables will reside in which registers (live values), and which variables will be spilled (insert load / store instructions). The register allocator is used when entering an off trace basic block / control flow within a region.)

Per claim 16:

- an instruction of said instructions which defines a value in said set of registers is not moved past said join instruction during said scheduling said instructions.

(Bharadwaj disclosed some instructions are not moved. As an example, col. 8, lines 59 & 66, identifies that an instruction may not move if resources (register not available to hold a value) are not available or if compensation code is not acceptable. A join instruction (col. 5, lines 14-27)

(an empty compensation block added prior to a block with many predecessors) requires acceptable compensation code entered into the compensation block (not moved past said join instruction).)

Per claim 19:

A system comprising:

-processor;

(Bharadwaj disclosed a CPU (col. 3, line 35).)

-a memory having a method of scheduling instructions therein, wherein upon execution of said method, said method comprises:

(Bharadwaj disclosed (Col. 3, line 39), "...memory..." and a scheduler (FIG. 5, #54).)

-allocating registers;

(Bharadwaj disclosed a register allocator, FIG. 5, #56.)

-building a trace comprising basic blocks;

(Bharadwaj disclosed a region builder (FIG. 6, #64), for determining a portion of the control flow diagram (trace) over which scheduling is performed. Col. 5, lines 1-17, regions are formed of basic blocks.)

-scheduling instructions within said trace after said allocating registers comprising:

(Bharadwaj disclosed scheduling after allocating registers at col. 4, lines 48-49.)

-moving a first instruction from a home block of said basic blocks to a destination block of said basic blocks;

(Bharadwaj disclosed moving a first instruction at col. 6, lines 42-43.)

generating compensation code comprising:

creating a compensation basic block;

(Bharadwaj disclosed creating a compensation basic block at col. 5, lines 24-27 (insert an empty compensation block).)

inserting a copy of said first instruction in said compensation basic block.

(Bharadwaj disclosed inserting a copy of said first instruction (compensation copy of the instruction) in said compensation basic block at col. 5, lines 50-52.)

Also, see limitations addressed in claims 1 & 11 above.

Per claim 30:

-compensation basic block is created between said off trace basic block and a successor block to said destination block.

(Bharadwaj disclosed that a compensation basic block is created anywhere that multiple predecessors in the control flow graph feed into a join block. See FIG. 13B, #109 (inserted

compensation block), used when considering a portion of the control flow diagram (col. 5, lines 1-27).)

Per claim 31:

-prior to generating compensation code, an incoming edge exists from said off trace basic block to said successor block.

(Bharadwaj disclosed an incoming edge (col. 5, lines 22-27), "any edge from a split block to a join block must be removed...by the insertion of an empty compensation block..." See FIGs. 13A & 13B. Incoming edges from Block A and Block B are removed from Block J (join block) and diverted through a compensation block (#107, #109) as shown in FIG. 13B.)

***Response to Arguments***

5. Applicant has argued, in substance, the following:

(A) As Applicant has noted, on page 10, last paragraph of Remarks, received 20 April 2005, "Smith teaches that register allocation, not instruction scheduling, may require spill code to be generated." Continuing on page 11, 2nd paragraph, Applicant recites that Smith fails to teach the limitations of claim 1.

Examiner's Response: New limitations have been added to claim 1, and similarly to all independent claims. The new limitations are addressed in the rejections above. New art describes a type of compensation code that correctly schedules code while preventing duplicate instruction scheduling along a control flow path (col. 5, lines 50-54).

6. Applicant's arguments with respect to claims 1, 12, 19, 28, and 29 have been considered but are moot in view of the new grounds of rejection.

***Conclusion***

7. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (571) 272-3704. The examiner can normally be reached Monday through Thursday, from 7:00 AM to 5:30 PM If

attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached at (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 through 15 July 2005. After 15 July 2005, the fax number will be 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary Steelman

07/06/2005

TED T. VO
primary Examiner